IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor :	Judy M. Gehman	
Appln. No.:	10/816,213	
Filed :	April 1, 2004	Group Art Unit: 2191
For :	SYSTEM AND METHOD FOR IMPLEMENTING MULTIPLE INSTANTIATED CONFIGURABLE PERIPHERALS IN A CIRCUIT DESIGN	Examiner: Satish Rampuria
Docket No.:	03-1002/L13.12-0246	

REPLY BRIEF FOR APPELLANT

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Mail Stop Appeal Brief-Patents
Commissioner for Patents
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Alexandria, VA 22313-1450

Sir:

This is in reply to the Examiner's Answer dated September 16, 2009, and in particular section (10) "Response to Argument" on pages 15 to 21.

Each subheading is addressed separately below.

1. Bowen Does Not Disclose Different Configurations Instantiated in a Single IC Chip Design

The Examiner refers to Bowen para. [0011] as somehow supporting that different configurations instantiated in a single IC chip design. However, para. [0011] supports Applicant's interpretation of the reference, not the Examiner's.

Bowen teaches using a configuration (without modification to that particular configuration) multiple times in a single chip design. Bowen does not disclose multiple instances of a peripheral device instantiated on the same IC with different configurations.

Bowen para. [0011] states,

> In one embodiment of the present invention, the function is a shared function. More particularly, the function in the FPGA is shared amongst all its uses. In another embodiment of the present invention, the configuration of the FPGA is duplicated for each use, so that the function is used as an inline function. In yet another embodiment of the present invention, the FPGA is configured to provide an array of functions, where N copies of the function are specified for use M times. (Emphasis added).

The first sentence tells us that a single, configured FPGA is shared by multiple uses. This sentence does not disclose two or more of the same FPGA instantiated on the same chip and configured differently from one another.

In the second sentence, Bowen states that "the configuration of the FPGA is duplicated for each use, so that the function is used as an inline function." In this embodiment, Bowen refers to a single configuration and a single function that is duplicated for each use. Again, this sentence does not disclose different configurations of the same FPGA instantiated on the same IC chip.

In the third sentence, Bowen describes "the FPGA is configured to provide an array of functions, where N copies of the function are specified for use M times." Again, it is the same function copied N times. Bowen does not disclose different configurations of the FPGA instantiated on the same IC chip.

So the Examiner's reliance on para. [0011] does not support the rejection.

2. Options are Not Selectable Without Modification To The Hardware Description

Applicants rely on their arguments provided in their main brief.

3. Bowen Does Not Disclose Selecting Between the Options at Compile Time for Each Instantiation of the Peripheral Device

The Examiner states that Applicant does not provide any reasoning for their arguments. However, The Examiner has admitted in the previous Office Action that Bowen does not

disclose "selecting between the options at compile time for each instance of the peripheral device such that at least two of the instances have different configurations from one another," as recited in claim 1. Applicant agrees, and Bowen in fact does not disclose these features.

4. Duboc et al. Fails to Disclose That Two Different Instantiations Can Have Two Different Configurations Selectable at Compile Time

Doboc et al. generally disclose a way to take existing building blocks and user input to make RTL (a hardware description), reduce to gates, and make an integrated circuit.

Duboc et al. do not disclose using the same building block more than once with different configurations in the same IC. Duboc mentions reusable templates, nowhere in Duboc does it say the same template is used multiple times with different inputs (configurations) in the same DSP.

Applicants rely on their detailed arguments regarding Duboc and the combination of Bowen and Duboc provided in their main brief.

5. Dependent Claims 2 and 3 (similarly claims 15, 17, 20)

In their main brief, Applicants stated they do not understand why the Examiner cited Bowen paragraph [0111] or how it applies to claim 2.

The Examiner suggested Applicants are "looking at the wrong paragraph" because for the limitations of claim 2, paragraph [0109] was cited, not paragraph [0111].

However, the Examiner cited BOTH paragraphs [0109] and [0111] in the rejection of claim 2. Neither supports the rejection.

Claim 2 adds that the step of selecting comprises "passing a parameter value to the function block at compile time for each instance of the hardware peripheral."

Starting at paragraph [0105] Bowen describe that parts of the design description allocated to hardware can be written by the designer using a register transfer level (RTL) design language. Paragraph [0109 simply states that,

> "RTL descriptions are passed straight through to the RTL synthesizer e.g. a Handel-C compiler."

This is the compiler that takes the C code (or RTL language) and creates the hardware description to put into the FPGA.

Paragraphs [0105] through [0111] have nothing to do with claim 2, wherein a parameter value is passed to a function block at compile time for each instance of a hardware peripheral, within the context of claim 1, where we have at least two instances of the peripheral device with different configurations from one another, wherein the options are selected without modification to the hardware description.

For claim 3, Applicants rely on their previous arguments.

6. **Claims "7 and 16", "4 and 12"**

Applicants rely on their previous arguments.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 23-1123.

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